Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2026

Second Semester

Applied Electronics

PAPT2421 - ANALOG AND MIXED SIGNAL IC DESIGN

Regulations - 2024

Duration: 3 Hrs. ***Maximum: 100 Marks***

PART – A(ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	Questions	BLT	CO	Marks
1.	List two challenges in analog design?	L1	1	2
2.	Compare the common gate stage and cascade stage in terms of gain and input impedance?	L2	1	2
3.	Identify the key steps in the submicron CMOS process flow?	L1	2	2
4.	Describe the effect of circuit noise on operational amplifier performance?	L2	2	2
5.	Define differential non-linearity in a Digital-to-Analog Converter?	L1	3	2
6.	Differentiate between Flash ADC and Pipeline ADC architectures?	L2	3	2
7.	Identify the different MOS transistor layers used in layout design?	L1	4	2
8.	Discuss the importance of matching in analog layout techniques?	L2	4	2
9.	Name two types of voltage-controlled oscillators?	L1	5	2
10.	Describe the role of a charge pump in a PLL?	L2	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No		Questions	BLT	CO	Marks
11.	a	Describe the structure and characteristics of MOSFETs?	L1	1	16
		Or			
	b	Outline the different stages of a single-stage amplifier and their functions?	L1	1	16
12.	a	Compare the different types of current mirrors used in analog circuit design?	L2	2	16
		Or			
	b	Illustrate how circuit noise affects Op-Amp performance and discuss ways to mitigate it?	L2	2	16
13.	a	Given a set of DAC specifications, determine the architecture that best suits the design requirements?	L3	3	16
		Or			
	b	Analyse the impact of clock jitter on ADC performance and propose methods to improve it?	L3	3	16

14.	a	Break down the different components of analog layout techniques and their significance in mixed-signal design?	L4	4	16
		Or			
	b	Examine the interconnection issues in mixed-signal layout and suggest possible design considerations to minimize them?	L4	4	16
15.	a	Assess the non-ideal effects in PLLs and their impact on system performance?	L5	5	16
		Or			
	b	Justify the selection of a specific oscillator architecture for frequency synthesis applications based on performance metrics?	L5	5	16

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